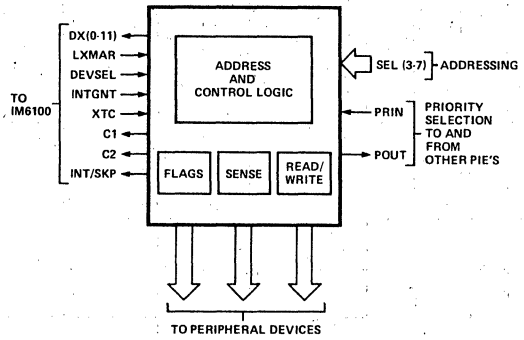
INTERSIL

IM6101
Programmable Interface Element (PIE)

FEATURES

- **Compatible with IM6100 Microprocessor**
- **Four Separate SENSE Input Lines to Sense the Status of Peripheral Devices**
- **Four Programmable OPERATE Control Lines for READ/WRITE on Peripheral Devices**
- **Four General Purpose FLAGS each of which is Programmable**
- **Chained Vectored Priority Interrupt Structure Possible**
- **Low Power: Less than 1mW @ 5V**
- **TTL Compatible at +5V**

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

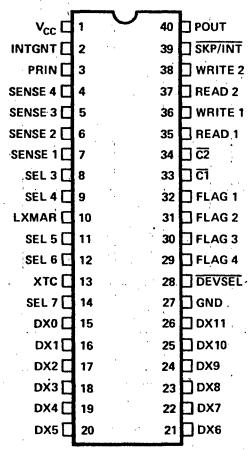


FIGURE 1.

GENERAL DESCRIPTION

The IM6101 is a Programmable Interface Element (PIE) device designed for interfacing various peripheral chips such as UART's, FIFO's, Keyboard Scanner's to IM6100 Microprocessor. In this way, the IM6101 eliminates the need for additional external logic between 6100 μP and its peripherals.

The IM6101 provides the control signals to peripheral devices for READING or WRITING on the DX bus by activating the WRITE CNTRL and READ CNTRL lines with IOT (Input Output Transfer) instructions.

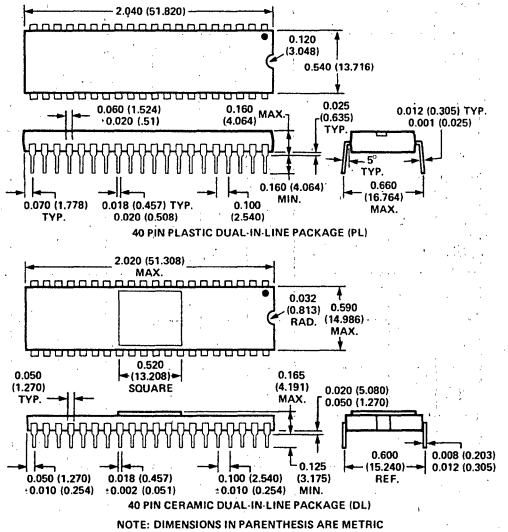
Each IM6101 can sample 4 status lines from peripheral devices. It can also generate interrupt requests to the μP if the corresponding individual interrupt enable bits in the PIE are enabled and the respective status lines become active.

The four FLAG lines may be set or reset under program control to send control information to the peripheral devices or to send binary data.

ORDERING INFORMATION

ORDER CODE	IM6101-1	IM6101A	IM6101
PLASTIC PKG.	IM6101-1IPL	IM6101-AIPL	IM6101-IPL
CERAMIC PKG.	IM6101-1IDL	IM6101-AIDL	—
MILITARY TEMP.	IM6101-1MDL	IM6101-AMDL	—
MILITARY TEMP. WITH 883B	IM6101-1 MDL/883B	IM6101-AMDL/ 883B	—

PACKAGE DIMENSIONS



IM6101 FUNCTIONAL DESCRIPTION

Pin Number	Symbol	Input/ Output	Description
1	V_{CC}		+5 volts
2	INTGNT	I	A high level on INTERRUPT GRANT inhibits recognition of new interrupt requests and allows the priority chain time to uniquely specify a PIE.
3	PRIN	I	A high level ON PRIORITY IN and an interrupt request will select a PIE for vectored interrupt.
4	SENSE 4	I	The SENSE input is controlled by the SL (sense level) and SP (sense polarity) bits of control register B. A high SL level will cause the SKIP flip flop to be set by a level while a low SL level causes sense and interrupt flip flops to be set by an edge. A high SP level will cause the sense flip flop to set by a positive going edge or high level. A high IE (interrupt enable) level generates an interrupt request whenever the INT flip flop is set (by an edge).
5	SENSE 3	I	See pin 4 — SENSE 4
6	SENSE 2	I	See pin 4 — SENSE 4
7	SENSE 1	I	See pin 4 — SENSE 4
8	SEL 3	I	Matching SELECT(3-7) inputs with PIE addressing on DX(3-7) during IOTA selects a PIE for programmed input output transfers.
9	SEL 4	I	See pin 8 — SEL 3
10	LXMAR	I	A positive pulse on LOAD EXTERNAL ADDRESS REGISTER loads address and control data from DX(3-11) into the address register.
11	SEL 5	I	See Pin 8 — SEL 3
12	SEL 6	I	See Pin 8 — SEL 3
13	XTC	I	The XTC input is a timing signal produced by the microprocessor. When XTC is high a low going pulse on DEVSEL initiates a "read" operation. When XTC is low, a low going pulse on DEVSEL initiates a "write" operation.
14	SEL 7	I	See Pin 8 — SEL 3
15	DX 0	I/O	Data transfers between the microprocessor and PIE take place via these input/output pins.
16	DX 1	I/O	See Pin 15 — DX 0
17	DX 2	I/O	See Pin 15 — DX 0
18	DX 3	I/O	See Pin 15 — DX 0
19	DX 4	I/O	See Pin 15 — DX 0
20	DX 5	I/O	See Pin 15 — DX 0
21	DX 6	I/O	See Pin 15 — DX 0
22	DX 7	I/O	See Pin 15 — DX 0
23	DX 8	I/O	See Pin 15 — DX 0
24	DX 9	I/O	See Pin 15 — DX 0
25	DX 10	I/O	See Pin 15 — DX 0
26	DX 11	I/O	See Pin 15 — DX 0
27	GND		
28	$\overline{DEVSEL}$	I	The DEVSEL input is a timing signal produced by the microprocessor during IOT instructions. It is used by the PIE to generate timing for controlling PIE registers and "read" and "write" operations.
29	FLAG 4	O	The FLAG outputs reflect the data stored in control register A. Flags (1-4) can be set or reset by changing data in CRA via a WRA (write control register A) command. FLAG1 and FLAG3 can be controlled directly by PIE commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.
30	FLAG 3	O	See Pin 29 — FLAG 4
31	FLAG 2	O	See Pin 29 — FLAG 4
32	FLAG 1	O	See Pin 29 — FLAG 4
33	$\overline{C1}$	O	The PIE decodes address, control and priority information and asserts outputs C1 and C2 during the IOTA cycle to control the type of data transfer. These outputs are open drain for bussing and require pullup resistors to V_{CC}. C1(L), C2(L) - vectored interrupt C1(L), C2(H) - READ1, READ3 or RRA commands C1(H), C2(H) - all other instructions
34	C2	O	See Pin 33 — C1
35	READ1	O	Outputs READ1 and READ2 are used to gate data from peripheral devices onto the DX bus for input to the IM6100. Note the data does not pass through the PIE.
36	WRITE1	O	Outputs WRITE1 and WRITE2 are used to gate data from the IM6100 DX bus into peripheral devices. Data does not pass through the PIE.
37	READ2	O	See Pin 35 — READ1
38	WRITE2	O	See Pin 36 — WRITE1
39	$\overline{SKP/INT}$	O	The PIE asserts this line low to generate interrupt requests and to signal the IM6100 when sense flip flops are set during SKIP instructions. This output is open drain.
40	POUT	O	A high level on priority out indicates no higher priority PIE interrupt requests are outstanding. This output is tied to the PRIN input of the next lower priority PIE in the chain.

TIMING DIAGRAM

Timing for a typical IOT transfer is shown in Figure 2. During the IFETCH cycle, the processor obtains from memory an IOT instruction of the form 6XXX. During the IOTA the processor places that instruction back on the DX lines ③ and pulses LXMAR transferring address and control information for the IOT transfer to all peripheral devices. A low going pulse on $\overline{\text{DEVSEL}}$ while XTC is high ④ is used by the addressed PIE along with decoded control information to generate $\overline{\text{C1}}$, $\overline{\text{C2}}$, $\overline{\text{SKP}}$ and controls for data transfers to the processor. Control outputs READ1 and READ2 are used to gate peripheral data to the DX lines during this time. A low going pulse on $\overline{\text{DEVSEL}}$ while XTC is low ⑤ is used to generate WRITE1 and WRITE2 controls. These signals are used to clock processor accumulator data into peripheral devices.

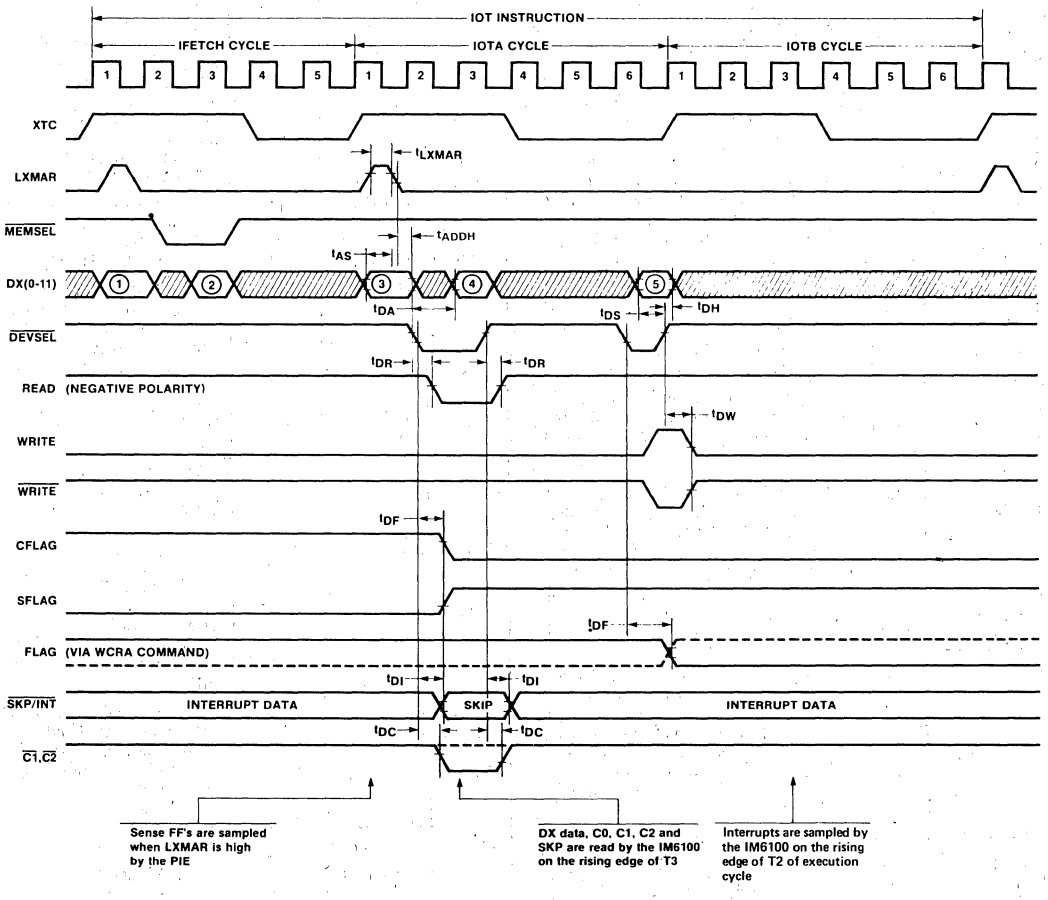


FIGURE 2. IM6101 PIE Timing Diagram.

All PIE timing is generated from IM6100 signals LXMAR, $\overline{\text{DEVSEL}}$, and XTC. No additional timing signals, clocks, or one shots are required. Propagation delays, pulse width, data setup and hold times are specified for direct interfacing with the IM6100.

PIE ADDRESS AND INSTRUCTIONS

The IM6100 communicates with the PIE and with peripherals through the PIE via IOT commands. During the IOTA cycle (See Figure 1) an instruction of the form 6XXX is loaded into all PIE instruction registers. The bits are interpreted as shown below.

The 5 address bits (3-7) are compared with the select inputs SEL3, SEL4, SEL5, SEL6, SEL7 to address 1 of 31 possible PIE's. Address zero is reserved for IOT's internal to the IM6100. The four control bits are decoded to select one of 16 instructions. Note also that the IOT instructions 66XX are reserved for the Parallel Input/Output Port (P10 - IM6103).

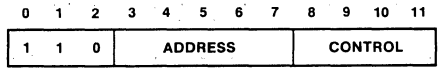


FIGURE 3. PIE Instruction Format.

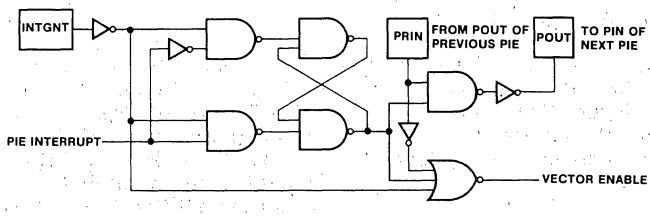
CONTROL	MNEMONICS	DESCRIPTION
0000 1000	READ1 READ2	The READ instructions generate a pulse on the appropriate read outputs. This signal is used by the peripheral device to gate data onto the DX bus to be "OR'ed" with the IM6100 accumulator data.
0001 1001	WRITE1 WRITE2	The WRITE instructions generate a pulse on the appropriate write output. This signal is used by peripherals to load the IM6100 accumulator data on the DX lines into peripheral data registers.
0010 0011 1010 1011	SKIP1 SKIP2 SKIP3 SKIP4	The SKIP instructions test the state of the sense flip flops. If the input conditions have set the sense flip flop, the PIE will assert the SKP/INT output causing the IM6100 to skip the next program instruction. The sense flip flop is then cleared. If the sense flip flop is not set, the PIE does not assert the SKP/INT output and the IM6100 will execute the next instruction.
0100	RCRA	The Read Control Register A instruction gates the contents of CRA onto the DX lines during time ④ to be "OR" transferred to the IM6100 AC. (See Figure 2)
0101 1101 1100	WCRA WCRB WVR	The Write Control Register A, Write Control Register B and Write Vector Register instructions transfer IM6100 AC data on the DX lines during time ⑤ of IOTA into the appropriate register. (See Figure 2) Bits 10, 11 of the VR;5, 7 of CRA; 8-11 of CRB are don't care bits for these instructions.
0110 1110	SFLAG1 SFLAG3	The SET FLAG instructions set the bits FL1 and FL3 in control register A to a high level. PIE outputs FLAG1 and FLAG3 follow the data stored in bits FL1 and FL3 of CRA.
0111 1111	CFLAG1 CFLAG3	The CLEAR FLAG instructions clear the bits FL1 and FL3 in control register A to a low level.
$(6007)_8$	CAF	IM6100 internal IOT instruction CLEAR ALL FLAGS clears the interrupt requests by clearing the sense flip flops. It has no effect on control register output flags FL1, FL2, FL3, FL4. To clear these output flags, bits 0-3 of CRA must be cleared using WCRA with bits 0-3 of AC cleared.

PRIORITY FOR VECTORED INTERRUPT

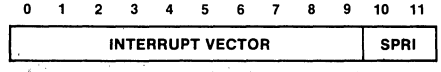
A hardware priority network uniquely selects a PIE to provide a vectored address. *The first IOT command of any type,* after the IM6100 signal INTERRUPT GRANT goes high, resets the line INTGNT to a low level. The signal INTGNT is used to freeze the priority network and enable vector generation. Within a given PIE, the internal priority is interrogated during every LXMAR.

The highest priority PIE has PRIN tied to V_{CC}. The lowest priority PIE is the last one on the chain. The vector address generated by the PIE consists of 10 bits from the vector register and two bits that indicate the sense input within the highest priority PIE that generated the interrupt.

A. Daisy-chaining of several PIE chips.



B. Interrupt Vector Register Format.



SPRI: Sense Priority

SPRI	Conditions*
00	SENSE1
01	SENSE2 and not SENSE1
10	SENSE3 and not (SENSE2 or SENSE1)
11	SENSE4 and not (SENSE3 or SENSE2 or SENSE1)

*All sense input lines are enabled for interrupts.

FIGURE 4. IM6101 Priority for Vectored Interrupt.

I/O CONTROL LINES (C1 AND C2)

The type of input-output transfer is controlled by the selected PIE by activating the $\overline{C1}$, $\overline{C2}$ lines as shown below. These outputs are open drain.

$\overline{C1}$	$\overline{C2}$	
H	H	DEV/PIE ← AC Write
L	H	AC ← AC + DEV/PIE "OR" Read
L	L	PC ← VECTOR ADDRESS Vectored Interrupt

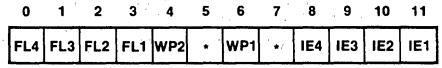
INTERRUPT/SKIP (INT/SKP)

Interrupt and skip information are time multiplexed on the same lines. Since the IM6100 samples skip and interrupt data at separate times (see Figure 1) there is no degradation in system performance. The PIE samples the sense flip flops and generates an interrupt request for enabled bits on the rising edge of LXMAR. Interrupt requests are asserted by driving the $\overline{INT/SKP}$ line low. During IOTA of SKIP instructions the INT/SKP reflects the SENSE flip flop data.

If the SENSE flip flop is set, the INT/SKP line is driven low to cause the IM6100 to skip the next instruction. This output is open drain.

CONTROL REGISTER A (CRA)

The CRA can be read and written by the IM6100 via the RCRA and WCRA commands. The format and meaning of control bits are shown below.



* Don't care for WCRA, 0 for RCRA

FIGURE 5. Format for Control Register A.

FL(1-4)

Data on FLAG outputs corresponds to data in FL (1-4). Changing the FL bits in CRA changes the corresponding FLAG output.

WP(1,2)

A high level on WRITE POLARITY bits causes positive pulses at the WRITE outputs (see Figure 1).

IE(1-4)

A high level on INTERRUPT ENABLE enables interrupts.

CONTROL REGISTER B

The CRB can be written by the IM6100 via the WCRB instruction. It has no read back capability. The format and meaning of control bits are shown below. Bits 8-11 are don't care bits.

0	1	2	3	4	5	6	7
SL4	SL3	SL2	SL1	SP4	SP3	SP2	SP1

FIGURE 6. Format for Control Register B.

SL(1-4)

A high level on the SENSE LEVEL bits causes the SENSE inputs to be level sensitive. A low level on the SL bits causes the SENSE inputs to be edge sensitive. The INT FFs are set only if a sense line is set up to be edge sensitive.

SP(1-4)

A high level on the SENSE POLARITY bits causes the SKIP flip flop to be set by a high level or positive going edge. A low level causes the SKIP flip flop to be set by a low level or negative going edge.

PERIPHERAL INTERFACE LINES

SENSE(1-4)

The IM6101 has two latches associated with each sense input — a SKIP flip flop and an INTERRUPT flip flop.

For the Interrupt flip flop to be set, the corresponding interrupt enable bit must be set to 'one'. If the sense input is programmed to be edge sensitive, the flip flop is set when the edge occurs. If it was initially programmed to be level sensitive and then the mode is changed to be edge sensitive, the flip flop will be set if the polarity of sense input line corresponds to its SP bit.

All conditions that set the Interrupt flip flop also set the associated Skip flip flop. In addition, the Skip flip flop is set when the polarity of the sense input corresponds to its SP bit in the level sensitive mode.

The Skip flip flop is cleared at IOTA READ time by executing a CAF (6007) instruction or a SKIP instruction on the associated sense input that actually skips. In the level sensitive mode, whenever the polarity of sense input does not correspond to its SP bit, the sense FF is cleared.

The Interrupt flip flop is cleared whenever the sense flip flop is cleared. In addition, it is cleared if the associated sense logic actually creates a vector, the interrupt enable bit is cleared to a 'zero' or the sense input is programmed to be level sensitive. Detailed operation of resetting Interrupt and Skip flop flops are as shown in Figure 7.

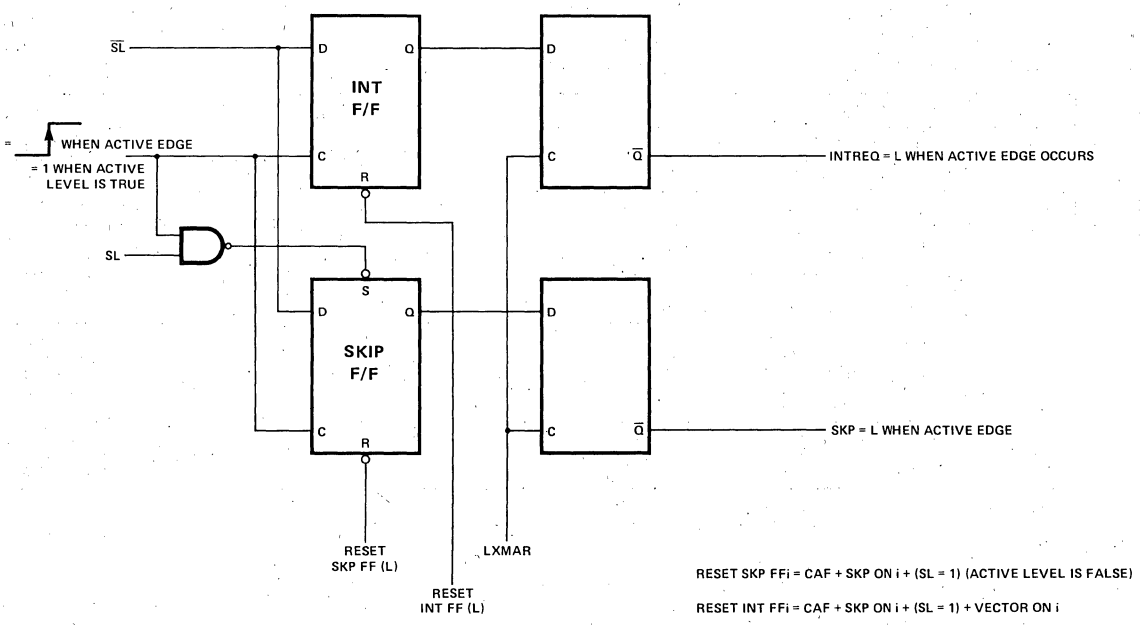


Figure 7. IM6101 SKIP Flip Flop and INTERRUPT Flip Flop Input Diagram.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6101A ..... -40°C to +85°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... 4.0V to 11.0V
Supply Voltage ..... +12.0V
Voltage On Any Input or
Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, T_A = -40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage	$GND \leq V_{IN} \leq V_{CC}$	-1.0		1.0	µA
4	V_{OH}	Output Voltage High	I_{OH} = 0mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			GND+0.01	V
6	I_{OL}	Output Leakage	$GND \leq V_{OUT} \leq V_{CC}$	-1.0		1.0	µA
7	I_{CC}	Power Supply Current—Standby	V_{CC}=10V±5%		1.0	500	µA
8	I_{CC}	Power Supply Current—Dynamic	V_{CC}=10V±5% f=571 kHz			2.0	mA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ±5%, T_A = -40°C to +85°C, C_L = 50pF

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{DR}	Delay from DEVSEL to READ			150	ns
2	t_{DW}	Delay from DEVSEL to WRITE	50		150	ns
3	t_{DF}	Delay from DEVSEL to FLAG			200	ns
4	t_{DC}	Delay from DEVSEL to C1, C2			215	ns
5	t_{DI}	Delay from DEVSEL to SKP/INT			215	ns
6	t_{DA}	Delay from DEVSEL to DX			215	ns
7	t_{LXMAR}	LXMAR Pulse Width	120			ns
8	t_{AS}	Address Setup Time	40			ns
9	t_{AH}	Address Hold Time	50			ns
10	t_{DS}	Data Setup Time	65			ns
11	t_{DH}	Data Hold Time	50			ns

Note: See Figure 2 for an A.C. Timing Diagram.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6101-1I ..... -40°C to +85°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... 4.0V to 7.0V
Supply Voltage ..... +8.0V
Voltage On Any Input or
Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage	GND≤V_{IN}≤V_{CC}	-1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = -0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OL}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	μA
7	I_{CC}	Power Supply Current—Standby	V_{CC} = 5V ± 10%		1.0	100	μA
8	I_{CC}	Power Supply Current—Dynamic	V_{CC}=5V±10% f=330 kHz			500	μA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -40°C to +85°C, C_L = 50pF

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{DR}	Delay from DEVSEL to READ			300	ns
2	t_{DW}	Delay from DEVSEL to WRITE	100		300	ns
3	t_{DF}	Delay from DEVSEL to FLAG			375	ns
4	t_{DC}	Delay from DEVSEL to C1, C2			460	ns
5	t_{DI}	Delay from DEVSEL to SKP/INT			460	ns
6	t_{DA}	Delay from DEVSEL to DX			460	ns
7	t_{LXMAR}	LXMAR Pulse Width	240			ns
8	t_{AS}	Address Setup Time	80			ns
9	t_{AH}	Address Hold Time	125			ns
10	t_{DS}	Data Setup Time	80			ns
11	t_{DH}	Data Hold Time	100			ns

Note: See Figure 2 for an A.C. Timing Diagram.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Military IM6101AM ..... -55°C to +125°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... 4.0V to 11.0V
Supply Voltage ..... +12.0V
Voltage On Any Input or
Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, T_A = -55°C to +125°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage	$GND \leq V_{IN} \leq V_{CC}$	-1.0		1.0	µA
4	V_{OH}	Output Voltage High	I_{OH} = 0mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			GND+0.01	V
6	I_{OL}	Output Leakage	$GND \leq V_{OUT} \leq V_{CC}$	-1.0		1.0	µA
7	I_{CC}	Power Supply Current—Standby	V_{CC}=10V±5%		1.0	500	µA
8	I_{CC}	Power Supply Current—Dynamic	V_{CC}=10V±5% f=571 kHz			2.0	mA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, T_A = -55°C to +125°C, C_L = 50pF

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{DR}	Delay from DEVSEL to READ			165	ns
2	t_{DW}	Delay from DEVSEL to WRITE	50		165	ns
3	t_{DF}	Delay from DEVSEL to FLAG			220	ns
4	t_{DC}	Delay from DEVSEL to C1, C2			240	ns
5	t_{DI}	Delay from DEVSEL to SKP/INT			240	ns
6	t_{DA}	Delay from DEVSEL to DX			240	ns
7	t_{LXMAR}	LXMAR Pulse Width	135			ns
8	t_{AS}	Address Setup Time	45			ns
9	t_{AH}	Address Hold Time	55			ns
10	t_{DS}	Data Setup Time	70			ns
11	t_{DH}	Data Hold Time	55			ns

Note: See Figure 2 for an A.C. Timing Diagram.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Military IM6101-IM ..... -55°C to +125°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... 4.0V to 7.0V
Supply Voltage ..... +8.0V
Voltage On Any Input or
Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage	$GND \leq V_{IN} \leq V_{CC}$	-1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = -0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OL}	Output Leakage	$GND \leq V_{OUT} \leq V_{CC}$	-1.0		1.0	μA
7	I_{CC}	Power Supply Current—Standby	V_{CC} = 5V ± 10%		1.0	100	μA
8	I_{CC}	Power Supply Current—Dynamic	V_{CC}=5V±10% f=330 kHz			500	μA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C, C_L = 50pF

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{DR}	Delay from DEVSEL to READ			330	ns
2	t_{DW}	Delay from DEVSEL to WRITE	100		330	ns
3	t_{DF}	Delay from DEVSEL to FLAG			415	ns
4	t_{DC}	Delay from DEVSEL to C1, C2			510	ns
5	t_{DI}	Delay from DEVSEL to SKP/INT			510	ns
6	t_{DA}	Delay from DEVSEL to DX			510	ns
7	t_{LXMAR}	LXMAR Pulse Width	265			ns
8	t_{AS}	Address Setup Time	90			ns
9	t_{AH}	Address Hold Time	140			ns
10	t_{DS}	Data Setup Time	80			ns
11	t_{DH}	Data Hold Time	110			ns

Note: See Figure 2 for an A.C. Timing Diagram.

APPLICATION

INTRODUCTION

The IM6101, Programmable Interface Element (PIE), provides a universal means of interfacing industry standard LSI devices and peripheral equipment controllers to the IM6100 Microprocessor.

The IM6100 configures each PIE for a specific interface during system initialization by programming the control registers within the PIE for write enable polarities, sense polarities, sense edges or levels, flag values and interrupt enables. On power-up, the registers will contain random bit patterns.

The data transfer between the IM6100 and the peripheral devices does not take place through the PIE. The programmable Interface Element provides the steering signals for data transfers. This approach was chosen since all the standard LSI elements such as Keyboard chips, UARTs, FIFOs, etc. have internal storage latches and they require only control signals to take data from the bus or to put data on the bus. If some user defined peripheral interfaces do not have these built-in storage elements, discrete CMOS or low power Schottky latches, or flip-flops, must be provided to store the data from the IM6100 until the peripheral device is ready to accept it and to latch data from the peripheral devices until the IM6100 asks for it.

INTERRUPT PROCESSING WITH PIE'S

The PIEs provide for a vectored priority interrupt scheme. Up to 31 PIEs may be chained to obtain 124 interrupt lines. The microprocessor will recognize, identify and start servicing the highest priority interrupt request within 36.6μs at 3.3MHz.

The INTREQ lines from all PIEs are wire-ANDed together. A PIE generates an interrupt request, if any one of its four sense lines, which are interrupt enabled, become active by driving the INTREQ line to the IM6100 low. If no higher priority requests are outstanding (RESET, CPREQ, HLT or DMAREQ), the IM6100 will grant the request at the end of the current instruction. The content of the Program Counter is deposited in location 0000_8 of the memory and the program fetches the next instruction from location 0001_8. The return address is hence available in location 0000_8. This address must be saved in a software stack if nested interrupts are allowed.

The IM6100 activates the INTGNT signal high when an INTREQ is acknowledged. The INTGNT is reset by executing any IOT instruction. The PIEs use the INTGNT signal to freeze the priority network and to uniquely specify the PIE with the highest priority interrupt request. The PIE with the highest priority request sends a unique vector address to the IM6100 when the processor executes the first IOT instruction after the INTGNT. The Interrupt II Prototyping System uses the IOT instruction VECT (6047) for Vectoring.

The 12-bit vector address generated by the PIE consists of 10 high order bits from the vector register, defined by the user during system initialization, and two low order bits which indicate the sense input that generated the interrupt. Therefore, if the instruction in location 0001_8 is VECT-6047_8, the processor will branch to 1 of 4 locations, depending on which of the sense lines within a PIE generated the request. Each one of these locations must contain a Jump instruction pointing to the specific service routine for the corresponding sense input. The 36.6μs interrupt acknowledge time at 3.3 MHz consists of 17μs (max) to recognize an interrupt request, 3.6μs to grant an interrupt request, 10μs to execute the VECT for vectoring and 6.0μs to execute a Jump instruction to a specific service routine.

Proper vectoring requires the following conditions:

1. The IM6100 must be enabled for interrupts with the ION command.
2. The INTGNT output of the IM6100 must be connected to the INTGNT of all the PIEs and the PRIN of the PIE with the highest priority must be connected to VCC and its PROUT should be connected to the PRIN of the PIE with the next highest priority and so on.
3. The IE bit of the sense line that is expected to generate the interrupt must be set to 1.
4. The sense line must be programmed to be edge sensitive. If a sense line is programmed to be level sensitive, it will not generate an INTREQ nor will it generate a vector.
5. The vector register of the PIE must be initialized with the proper vector. Note that the two least significant bits are generated by the PIE itself.
6. The $\overline{C1}$ and $\overline{C2}$ lines of all the PIEs must be wired together with the $\overline{C1}$ and $\overline{C2}$ of the IM6100 and pull up resistors must be provided on these lines since the PIE $\overline{C1}$ and $\overline{C2}$ outputs are open drain. The $\overline{SKP/INT}$ line of the PIE must be wired with the INT and SKP lines of the IM6100. If the PIE DX lines are buffered, the external bus must be enabled onto the PIE DX with the XTB being active high and the PIE DX bus must be enabled onto the external bus when the C1 line of a PIE is active low (during RCRA, READ1, READ2 or vector).
7. The vector address will be generated with the first IOT of any kind after the INTGNT.
8. Note also that a successful skip on a sense line will reset an interrupt request by the sense line, if any. One should not thus turn on the interrupt system after a successful skip on a sense line expecting that the sense line that was just tested will generate a request.

SKIP HANDLING WITH PIE'S

Each PIE provides for four SENSE lines. The active state of the SENSE inputs can be programmed to be a low level, high level, positive edge or negative edge. There is a SENSE FF in the PIE associated with each SENSE line. This FF is set when the SENSE line is "active"

The state of the SENSE FF can be tested by the SKP commands. When the IM6100 executes a SKIP instruction, it will skip the next sequential instruction if the SENSE FFi is set. If the skip is successful, the FF will be cleared.

If the sense line was set up to be edge sensitive, it can, therefore, be tested for the 'set' state only once. If the FF is set by a level, it will be cleared by the successful skip and then, set immediately by the active level.

If the SENSE FF was set by an edge, and the respective IE bit is enabled, the PIE will generate an INTREQ to the IM6100. Provided the priority conditions are met, the PIE will supply the vector address to the IM6100 when it executes the first IOT instruction of any kind, after the INTREQ has been granted. If the vector address is generated by FFi, one may still skip once on sense line i.

It should be noted that if priority vectoring is inhibited by grounding PRIN, an INTREQ will be cleared only if a SKIPi instruction is executed to test the FFi that generated the request. Note also that an INTREQ will not be generated if the sense line was set up to be level sensitive.

In certain instances, one may be interested in restoring the set state of a SENSE FF after it has been successfully tested and cleared and if the SENSE line has been programmed to be edge sensitive. For example, assume that SENSE1 is programmed to be positive edge sensitive (SL1 = 0, SP1 = 1). The transition from a 0 to 1 occurred; SENSE FF1 is set; SENSE1 is at a 1 level. SKIP1 instruction will clear SENSE FF1. The SENSE FF1 can be set, under program control, by creating an internal edge. This is accomplished, in this specific instance, by programming SP1 to a 0 and then back to a 1. Since SP1 is in CRB and it cannot be read from the PIE, the CRB constant must be stored in user memory, for example, location KCRB.

```
        CLA
        TAD KCRB    /Get CRB constant
        AND K7740   /SP1 = 0
        WCRB        /Write CRB to clear SP1
        TAD K0020   /SP1 = 1
        WCRB        /Write CRB to set SP1

KCRB,   CRB         /CRB constant
        K7740, 7740
        K0020, 0020
```

Software systems employing Skip's on a Sense input while allowing the same input to create an Interrupt should pay attention to the fact that the Skip and Interrupt flip flops are synchronized by LXMAR from the IM6100. Since there is no LXMAR during IOTB of an I/O instruction, the following can occur. Assume that the following two instruction sequence is used:

```
SKIP SENSEX     /SENSE F/F SET?
JMP  -1         /NO: WAIT FOR IT
```

Where SENSEX is also Interupt enabled.

Now, assume that the appropriate 'Edge' occurs during the fetch state of the Skip instruction. The Edge causes both flip flops to be set and the LXMAR produced at IOTA time creates an Interrupt request. The Skip instruction execution causes a Skip and clears the Skip flop flop. However, the Interrupt flip flop will not reflect the fact that the Skip flip flop has been cleared until after the next LXMAR occurs. So, the Interrupt request remains active during IOTB time since the IOTB cycle does not have a LXMAR. The IM6100 honors the Interrupt request since the next LXMAR doesn't occur until after the IOT is finished. The Interrupt servicing routine will not Skip again if it tries to find the device that created the Interrupt. Note that the proper Vector Address will still be generated.

PIE INSTRUCTION FORMAT

The IM6100 communicates with the PIEs using the Input-Output Transfer (IOT) instructions. The first three bits, 0-2, are always set to 6_8 (110) to specify an IOT instruction. The standard PDP-8/E™ convention is to set the next 6 bits, 3-8, to specify 1 of 64 I/O devices and then to control the operation of the selected I/O device by using bits 9-11. However, the PDP-8/E interfaces are not standardized since a specific pattern of bits 9-11 could specify completely different operations in different I/O devices. For example, the pattern 000 in bits 9-11 could mean a read operation for Interface A, a write operation for Interface B, a skip instruction for Interface C and so on since the operation for any IOT instruction depends entirely upon the circuitry designed into the I/O device interface.

The IOT instruction format for the PIE is different from that used by PDP-8/E™ interfaces. The first three bits are, as usual, set to 6_8 to indicate an IOT instruction. The next 5 bits, 3-7, specify 1 of 31 PIEs and then the operation of the selected PIE is controlled by bits 8-11 in 16 uniquely specified ways. For example, the specific pattern 0000 in bits 8-11 means exactly the same operation for all PIEs, namely activate READ1 line.

Of the 32 possible combinations of bits 3-7, the pattern 00000 is reserved for internal Processor IOT instructions and hence not available as a PIE address.

Recommended address assignments for the IM6101-PIE (Programmable Interface Element) are as follows:

000	00	Internal IOT (600X) and DEC HS RDR (601X)
000	01	DEC HS PUNCH (602X) and DEC TTY Keyboard (603X)
000	10	DEC TTY PRINTER (604X)
000	11	INTERCEPT PIE-UART Serial Interface
001	00	INTERCEPT PIE-UART PRINTER Interface
001	01	IM6102-MEDIC REAL TIME CLOCK
001	10	Reserved for Intercept Option - 1
001	11	Reserved for Intercept Option - 2
010	00	IM6102-MEDIC EMC/DMA
010	01	IM6102-MEDIC EMC/DMA
010	10	IM6102-MEDIC EMC/DMA
010	11	IM6102-MEDIC EMC/DMA
011	00	IM6103-PIO
011	01	IN6103-PIO
011	10	IN6103-PIO
011	11	IN6103-PIO
100	00	USER
100	01	USER
100	10	USER
100	11	USER
101	00	USER
101	01	USER
101	10	USER
101	11	USER
110	00	USER
110	01	USER
110	10	USER
110	11	USER
111	00	Reserved for Intercept Option - 5
111	01	Reserved for Intercept Option - 4
111	10	Intercept FLOPPY DISK System (675X)
111	11	Reserved for Intercept Option - 3

PARAMETER	DEFINITION
Minimum Peripheral device write data setup time w.r.t. leading edge of WRITE	t_{WPD} (IM6100) + $t_{DW\ (MIN)}$ (IM6101) - t_{DSD} (IM6100)
Minimum Peripheral device write data hold time w.r.t. leading edge of WRITE	t_{DHD} (IM6100) + t_{WPD} (IM6100) - $t_{DW\ (MAX)}$ (IM6101)
Maximum Peripheral device read data enable time	t_{END} (IM6100) - t_{DR} (IM6101)

TIMING REQUIREMENTS ON PERIPHERAL DEVICES

The timing required on peripheral devices is affected by the combined delays of the IM6100 and IM6101 devices. The table above describes the peripheral device timing requirements with respect to the data given for the IM6100 and IM6101 AC characteristics.

The values at any operating frequency, temperature and/or power supply voltage can be evaluated by substituting the calculated values for the IM6100 and IM6101 parameters in the defining expressions.

ASYNCHRONOUS SERIAL INTERFACE WITH PIE AND UART

The IM6402/03 Universal Asynchronous Receiver/Transmitter is a general, purpose programmable serial device for interfacing an asynchronous serial data channel to a parallel synchronous data channel. The receiver converts a serial word with start, data, parity and stop bits to a parallel data word and checks for parity, framing and data overrun errors. The transmitter section converts a parallel data word into a serial word with start, data, parity and stop bits. The data word length may be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The number of stop bits may be 1 or 2 or 1 1/2 when transmitting a 5 bit code.

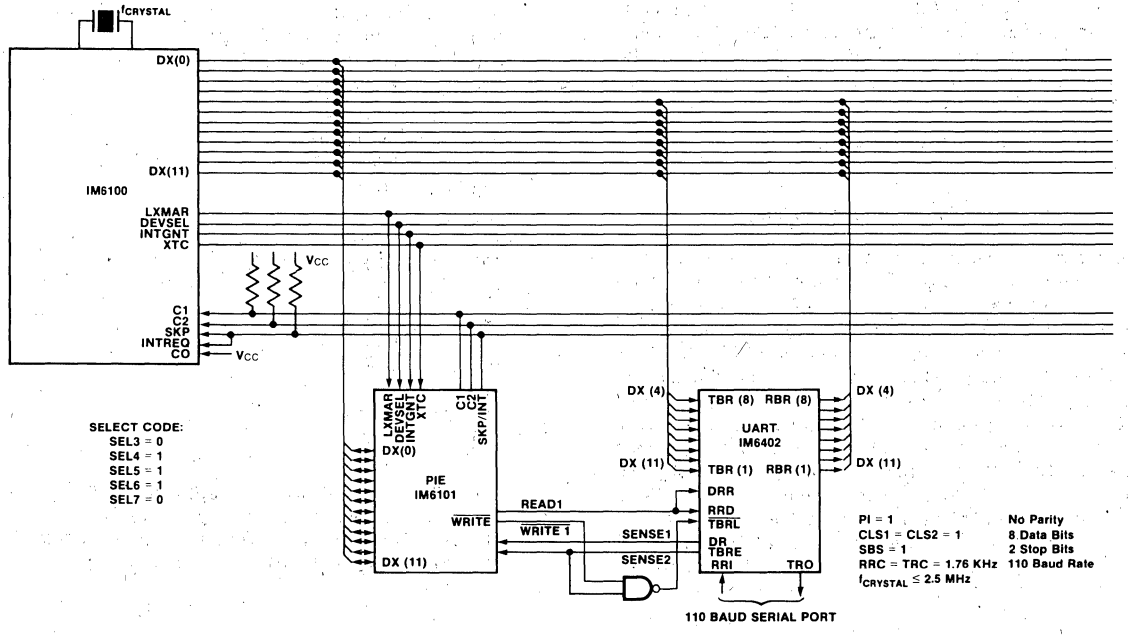
The IM6402/03 can be used in a wide variety of applications including interfacing modems, Teletype™ and remote data acquisition systems to the IM6100 microprocessor. The IM6403 makes provisions for a crystal oscillator and internal divider chain to specify the data transfer rate. In the IM6402 the data transfer rate is controlled by an external timing source, for example, a Baud Generator.

A functional block diagram of the PIE/UART/IM6100 interface is shown below. The UART is configured, in this specific example, to interface with an ASR-33 Teletype which has a data format that consists of 11 bits — a start bit, 8 data bits and 2 stop bits. The UART is clocked at 16X the data rate. For the 10 character per second ASR-33, the UART clock frequency would be 1.76 KHz.

An 8-bit data word from the IM6100 Accumulator is loaded into the Transmitter Buffer Register via inputs TBR8-TBR1 when the Transmit Buffer Register Load (TBRL) signal makes a zero to one transition. A high level on Transmit Buffer Register Empty (TBRE) indicates that the buffer is ready to accept a new character for transmission. The microprocessor checks the status of TBRE via SENSE2 before it transmits a new character to the UART by pulsing WRITE1. The start bit, data bits and stop bits appear serially at the Transmit Register Output (TRO).

A serial data stream on the Receiver Register Input (RRI) is clocked into the Receive Buffer Register. A high level on Data Received (DR) indicates that a character has been received. The contents of Receiver Buffer Register appear on the outputs RBR8-RBR1 when a low level is applied to Receiver Register Disable (RRD) input. The RBR outputs are tristated when RRD is high. A low level on Data Received Reset (DRR) clears the DR flag. RRD and DRR

PIE/UART/IM6100 INTERFACE

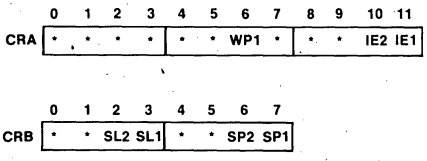


may be tied together to clear DR as the register data is being read. The microprocessor monitors the status of the DR flag via SENSE1 to see if a new character has been received before it reads the information stored in the buffer register by pulsing READ1 low.

The UART interface uses only the low order 8 bits of the IM6100 data bus (DX) to receive and transmit characters.

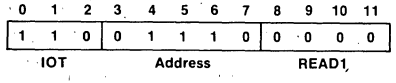
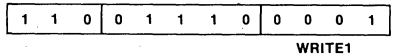
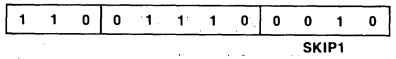
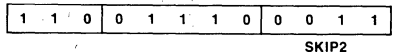
The NAND gate is used to load the UART with the leading edge of the WRITE pulse since the IM6100 data is valid only with respect to the leading edge at higher operating frequencies.

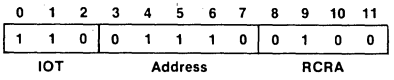
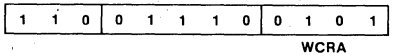
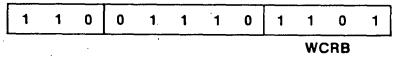
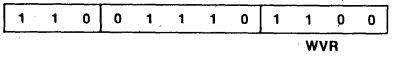
PIE CONTROL REGISTER ASSIGNMENTS FOR IM6402 UART INTERFACE:



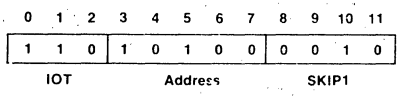
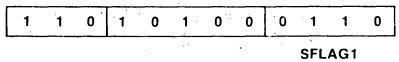
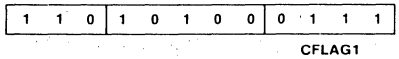
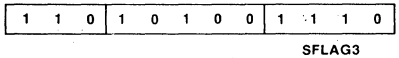
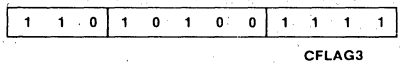
WP1 = 0	Active low WRITE1 (TBRL)
IE2 = 1	Interrupt enable for SENSE2 (TBRE)
IE1 = 1	Interrupt enable for SENSE1 (DR)
	If vectored interrupts are used (PIN = 1 or is part of a priority chain) the Interrupt Vector Register must be loaded with the desired vector address.
SL2 = 0; SP2 = 1	SENSE2 (TBRE) active on 0 to 1 transition
SL1 = 0; SP1 = 1	SENSE1 (DR) active on 0 to 1 transition

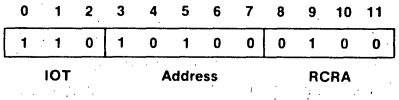
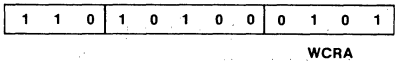
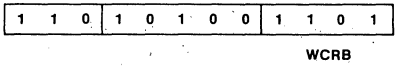
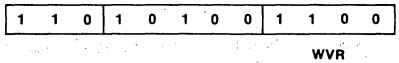
PIE ADDRESS AND CONTROL ASSIGNMENTS:

EXTERNAL COMMANDS	OCTAL CODE	DESCRIPTION
	6340	Activate RRD low to transfer Receiver Register contents onto the DX lines and clear the Data Received Flag.
	6341	Activate TBRL low to transfer data from the DX lines to the Transmit Buffer Register.
	6342	Skip the next instruction if the internal SENSE FF1 was set by a positive transition on Data Received (DR) and then clear SENSE FF1.
	6343	Skip the next instruction if the internal SENSE FF2 was set by a positive transition on Transmit Buffer Register Empty (TBRE) and then clear Sense FF2.

INTERNAL COMMANDS	OCTAL CODE	DESCRIPTION
	6344	'OR' transfer Control Register A to the AC.
	6345	Transfer AC to Control Register A
	6355	Transfer AC to Control Register B
	6354	Transfer AC (0-9) to Vector Register (0-9)

PIE Address and Control Assignments:

EXTERNAL COMMANDS	OCTAL CODE	DESCRIPTION
	6502	Skip and clear if SENSE1 is low — used to detect the status of the receive line.
	6506	Set FLAG1 to put the transmit line high ("MARK")
	6507	Clear FLAG1 to put the transmit line low ("SPACE")
	6516	Set FLAG3 to enable the paper tape reader
	6517	Clear FLAG3 to disable the paper tape reader

INTERNAL COMMANDS	OCTAL CODE	DESCRIPTION
	6504	'OR' transfer Control Register A to AC
	6505	Transfer AC to Control Register A
	6515	Transfer AC to Control Register B
	6514	Transfer AC (0-9) to Vector Register (0-9)

Subroutines for programmed IOT transfers:

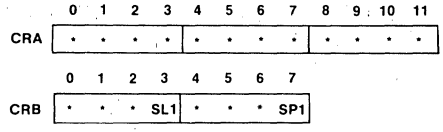
Program Listing:

```
                        /REFER TO THE APPLICATION BULLETIN M008
                         /"ROM BASED SUBROUTINE CALLS WITH THE
                         /IM6100" FOR THE IMPLEMENTATION OF A
                         /SOFTWARE STACK. THE ROUTINES IN THIS
                         /NOTE ASSUME THAT THE SUBROUTINES
                         /ARE RESIDENT IN RAM AND ARE CALLED BY
                         /THE CONVENTIONAL JMS INSTRUCTION.


                        *3200

                        /INPUT-OUTPUT ROUTINES FOR UART
                         /INPUT ROUTINE READS AN 8-BIT CHAR
                         /FROM THE UART INTO THE AC RIGHT
                         /JUSIFIED. THE OUTPUT ROUTINE XMTS
                         /A CHAR FROM THE AC TO THE UART AND
                         /THEN CLEARS THE AC.
                                /USER DEFINED MNEMONICS
                                RUART=6340      /READ UART DATA
                                WUART=6341      /WRITE UART

                                SKPDR=6342      /SKP IF DATA RECD
                               SKPTBR=6343      /SKP IF XMT RDY

3200  0000  INPUT,  0                          /ENTRY FOR SUBROUTINE
3201  6342         SKPDR
3202  5201         JMP .-1                     /WAIT FOR DATA READY

3203  7200         CLA
3204  6340         RUART                       /AC<= UART
3205  0207         AND K0377                   /STRIP 0-3
3206  5600         JMP I INPUT                 /RETURN

3207  0377  K0377, 0377



3210  0000  OUTPUT, 0
3211  6343         SKPTBR
3212  5211         JMP .-1                     /WAIT FOR XMT RDY

3213  6341         WUART
3214  7200         CLA                         /WRITE UART & CLA
3215  5610         JMP I OUTPUT                /RETURN
```

TELETYPE INTERFACE WITH PIE

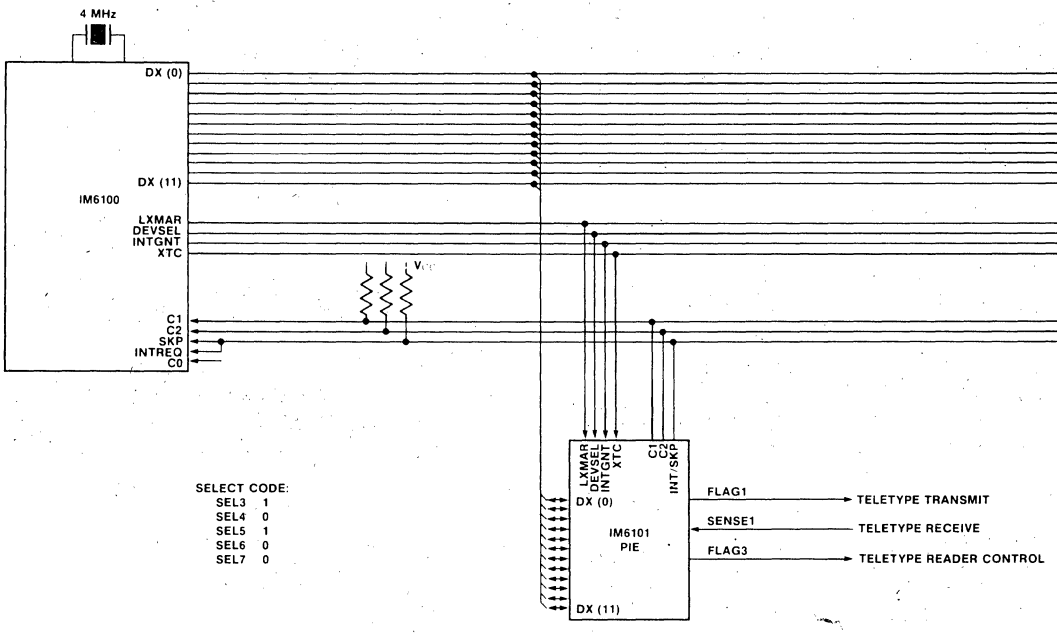
A simple economical program controlled serial interface for a Teletype can be built using only the Programmable Interface Element. The interface uses one Sense line to receive serial data, one Flag line to transmit serial data and one Flag line to control the Teletype paper tape reader, as shown below. Timing for proper transmit pulse widths, setting and clearing FLAG1, and proper receiver sampling times, testing SENSE1, is created via software timing loops.

PIE Control Register Assignments



SL1 = 1; SP1 = 0 SENSE1 is level sensitive and active low.

IM6100/PIE/TELETYPE INTERFACE



Subroutines for programmed IOT transfers:

Transmit character routine:

The transmit routine takes an 8-bit character from the Accumulator and transmits it to the Teletype via FLAG1. FLAG1 is initially set high or "mark". For each character, the program sends out a start bit ("space" - zero), 8 data bits with the least significant bit first and 2 stop bits ("mark" - one).

Program listing:

```
                                /TELETYPE XMT ROUTINE
                                 /FLAG1 IS INITIALISED TO 1(MARK)
                                 /CHAR TO BE XMTED IN AC4-11
                                 /NOMINAL BIT TIME 9.09 MS
                                 /4MHZ OPERATION FOR IM6100
                                 /AC AND L CLEARED AFTER XMT

                                        /USER DEFINED MNEMONICS

                                        TMARK=6506      /XMT MARK (1)
                                        TSPACE=6507     /XMT SPACE(0)

                                *3000

3000  0000  XMT,     0
3001  3160           DCA TEMP1        /SAVE AC
3002  1235           TAD M8
3003  3161           DCA TEMP2        /-8 IN TEMP2
3004  1160           TAD TEMP1        /RESTORE AC

3005  6507           TSPACE           /START BIT
3006  4225           JMS DELAY        /TIME OUT BIT

                                /XMT 8 DATA BITS LSB FIRST
3007  7010  LOOP,    RAR              /XMT BIT IN L
3010  7430           SZL
3011  5214           JMP .+3          /JMP IF 1

3012  6507           TSPACE           /XMT 0
3013  7410           SKP

3014  6506           TMARK            /XMT 1

3015  4225           JMS DELAY        /TIME OUT BIT
                                      /9.082 MS NOMINAL <.1% ERROR

3016  2161           ISZ TEMP2
3017  5207           JMP LOOP         /XMT 8 BITS

3020  6506           TMARK            /STOP BIT
3021  4225           JMS DELAY
3022  4225           JMS DELAY        /2 STOP BITS

3023  7300           CLA CLL
3024  5600           JMP I XMT        /RETURN

3025  0000  DELAY,   0000             /9.043 MS
3026  3160           DCA TEMP1        /SAVE AC
3027  1236           TAD M693
3030  3162           DCA TEMP3        /-693 IN TEMP3
3031  1160           TAD TEMP1        /RESTORE AC

3032  2162           ISZ TEMP3
3033  5232           JMP .-1          /TIME OUT LOOP
                                      /9.009 MS

3034  5625           JMP I DELAY      /RETURN

3035  7770  M8,      7770
3036  6513  M693,    6513

                     *160
0160  0000  TEMP1,   0000
0161  0000  TEMP2,   0000
0162  0000  TEMP3,   0000
```

Receiver character routine:

The receive routine accepts a serial data string from the Teletype which consists of a start bit, 8 data bits with the least significant bit first and 2 stop bits and assembles them, right justified, into an 8-bit word in the Accumulator. Each bit is sampled in the middle of the bit interval. The user can read character by character from the Teletype reader by turning the reader off after receiving each character and then reenabling it under program control to fetch the next character in sequence The routine assumes that the program is waiting for a character from the Teletype.

Program listing:

```
                        *3100
                        /TELETYPE RECEIVE ROUTINE
                         /SENSE1 IS INITIALISED TO BE LEVEL
                                 /SENSITIVE AND ACTIVE LOW
                         /AC AND L ARE CLEARED. CHAR IN AC 4-11

                                 /USER DEFINED MNEMONICS

                                 SKPLOW=6502      /SKP IF TTY IN IS 0
                                 RDRON=6516       /ENABLE RDR
                                 RDROFF=6517      /RDR OFF

3100  0000  RCVE,   0000
3101  7300          CLA CLL
3102  1235          TAD M8
3103  3161          DCA TEMP2        /-8 IN TEMP2

3104  6516          RDRON            /ENABLE RDR

3105  6502  START,  SKPLOW
3106  5305          JMP .-1          /WAIT FOR START BIT

3107  1330          TAD M349
3110  3162          DCA TEMP3        /-349 IN TEMP3

3111  2162          ISZ TEMP3
3112  5311          JMP .-1          /1/2 BIT DELAY
                                     /4.532 MS

3113  6502          SKPLOW
3114  5305          JMP START        /FALSE START BIT

3115  6517          RDROFF           /GOOD START BIT
                                     /TURN OFF RDR
3116  4225  DATA,   JMS DELAY       /FULL BIT DELAY TO THE
                                     /MIDDLE OF NEXT BIT
                                     /<.15% ERROR
3117  7100          CLL
3120  6502          SKPLOW
3121  7020          CML              /L=1 IF MARK
3122  7010          RAR

3123  2161          ISZ TEMP2
3124  5316          JMP DATA         /RCVE 8 BITS

3125  7012          RTR
3126  7012          RTR              /RIGHT JUSIFY

3127  5700          JMP I RCVE       /RETURN

3130  7243  M349,   7243
```